BEE 271 Spring 2017
Homework 4

Please answer the following questions. Each is worth 8 points.

1. Write a Verilog module using a casex statement that takes a 4-bit value as input and outputs the number of leading 1's, e.g., 0111 → 0, 1011 → 1, 1100 → 2, etc.

2. Create a module in Verilog that adds a 4-bit unsigned binary number to an 8-bit unsigned binary number, producing a 10-bit unsigned result using the + operator.

3. Create a module in Verilog that adds a 4-bit signed binary number to an 8-bit unsigned binary number, producing a 10-bit signed result using the + operator.

4. What is Shannon's expansion? What is a cofactor?

5. Implement F = A B C' + A B' D' using a 16:1 multiplexer.

6. Implement your 16:1 multiplexer solution to F = A B C' + A B' D' as directly as you can in Verilog using a case statement and the concatenation operator.

7. Use Shannon's expansion to implement F = A B C' + A B' D' using a 2:1 multiplexer, two NOR gates and one inverter. Show your steps.

8. Draw a schematic that implements F = A B C' + A B' D' using NAND gates and inverters. Will it have a hazard? If there is a hazard, will it be a static 1 or a static 0 hazard and how could you fix the formula and your circuit to eliminate the hazard?

9. Implement F = (A + B' + D') (A' + B' + C') using a 16:1 multiplexer.

10. Use Shannon's expansion to implement F = (A + B' + D') (A' + B' + C') using a 2:1 multiplexer and two NAND gates. Show your steps.

11. Use Shannon's expansion to implement F = (A + B' + D') (A' + B' + C') using a 4:1 multiplexer and two inverters. Show your steps.

12. Draw a schematic that implements F = (A + B' + D') (A' + B' + C') using NOR gates and inverters. Will it have a hazard? If there is a hazard, will it be a static 1 or a static 0 hazard and how could you fix the formula and your circuit to eliminate the hazard?